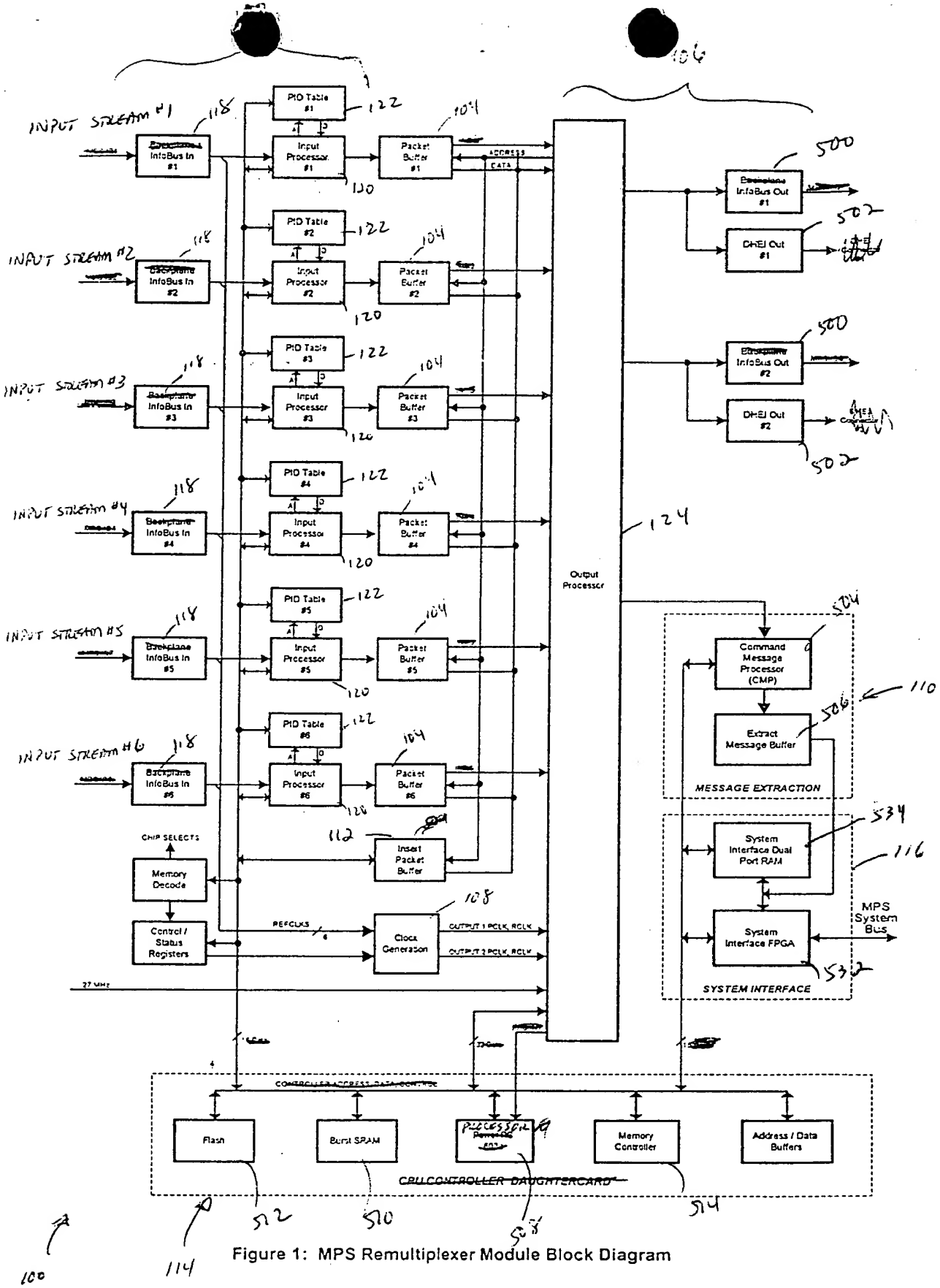

Figure 1: MPS Remultiplexer Module Block Diagram

FIG. 1

Figure 3: IP FPGA Block Diagram
(1 of 6 IP Channels Shown)

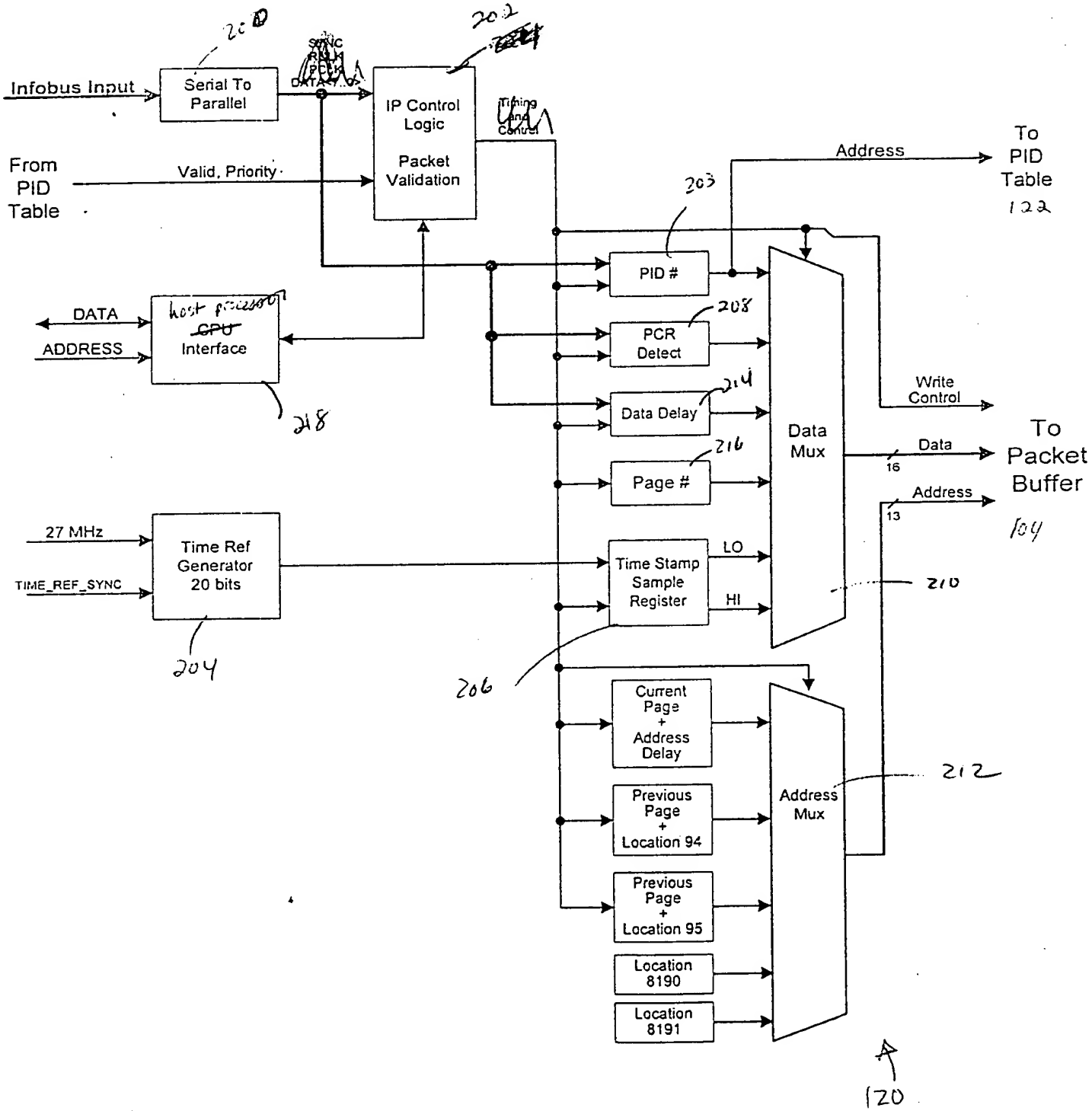

FIG. 2

Figure 5. Input PID Table

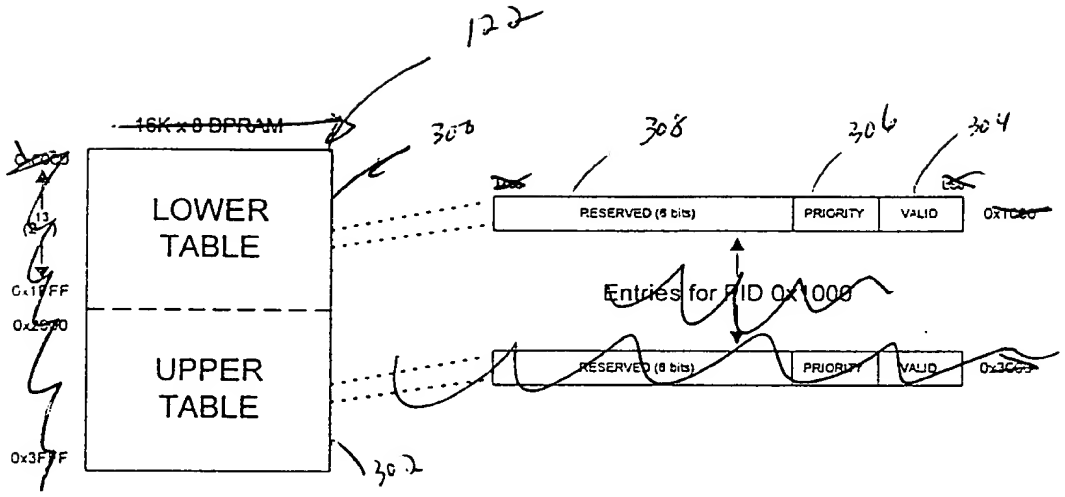

FIG. 3

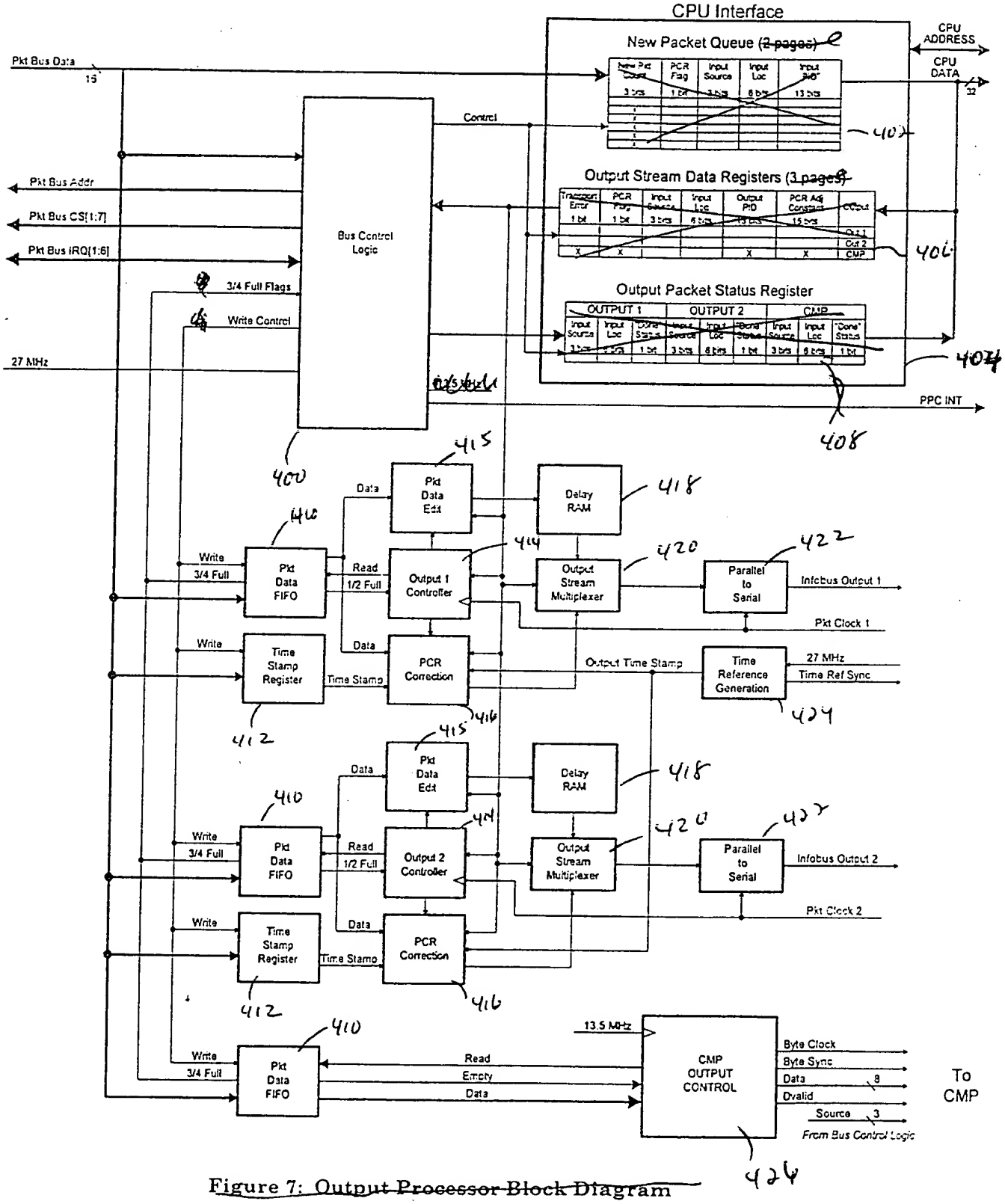

Figure 7: Output Processor Block Diagram

FIG. 4

Figure 10: Simplified ISR Flowchart

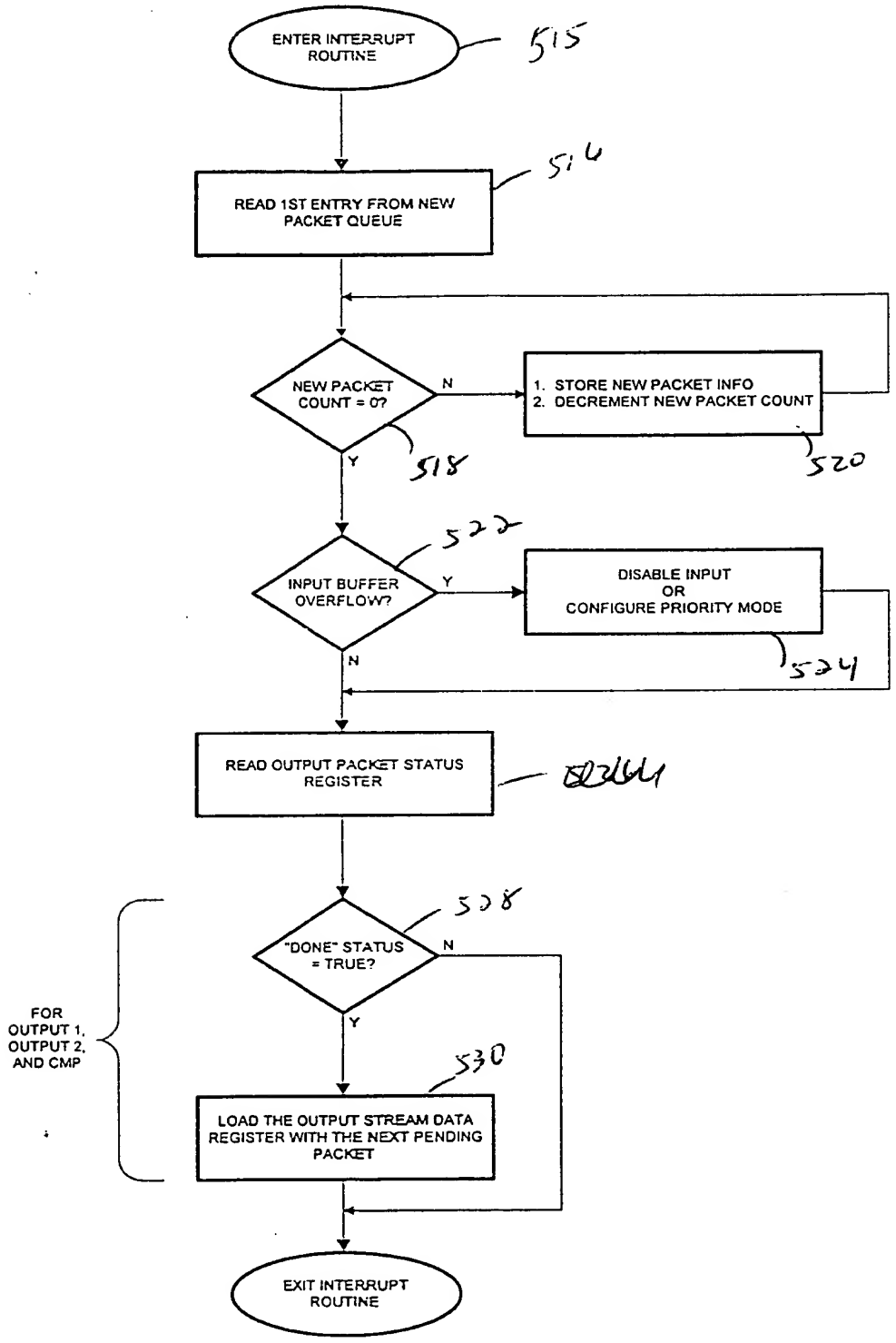

FIG. 5